	L #	Hits	Search Text	DBs	Time Stamp
1	L1	856	(scrub or scrubbing) and plasma and (etch or etching) and semiconductor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
2	L2	407	photoresist and L1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
3	L3	42802	(plasma adj etch) or (plasma adj etching)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
4	L4	364	L3 and L1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	207	photoresist and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
6	L6	21460	photoresist same plasma	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
7	L7	364	L1 and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
8	L8	4747	low-k	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15

	L #	Hits	Search Text	DBs	Time Stamp
9	L10	10	wet and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:15
10	L9	12	L8 and L7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:18
11	L12	234	((scrub or scrubbing) and plasma and (etch or etching) and semiconductor) and (photoresist same plasma)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:19
12	L13	300	((scrub or scrubbing) and plasma and (etch or etching) and semiconductor) and ((photoresist or P/R or resist) same plasma)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:20

	L #	Hits	Search Text	DBs	Time Stamp
13	L14	42147	(low-k or (low near2 dielectric))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:20
14	L15	55	14 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:20
15	L16	42	15 and ((@ad<"20011227") or (@rlad<"20011227"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:32
16	L17	270	("NH.sub.4OH" or "H.sub.2O.sub.2") near4 (deionized or DI)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:46

	L #	Hits	Search Text	DBs	Time Stamp
17	L18	495916	(fluorosurfactants or hydrocarbon)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:34
18	L19	32	17 and 18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:34
19	L20	5	19 and (brush or brushing or brushed or scrub$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:40
20	L21	175	Lam adj Research adj Corp$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:39

	L #	Hits	Search Text	DBs	Time Stamp
21	L22	3	21 and 17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:39
22	L23	19	21 and (brush or brushing or brushed or scrub$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:40
23	L24	4	17 and 438/?	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:49
24	L25	25	(scrub or scrubbing) near4 (wetting near agent)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:50

	L #	Hits	Search Text	DBs	Time Stamp
25	L26	4221	(chemical near4 clean)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:51
26	L27	80	26 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:51
27	L28	1	27 and 438/?.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 09:53
28	L29	756	(438/691).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:03

	L #	Hits	Search Text	DBs	Time Stamp
29	L31	1228	wafer near4 (Scrub$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:04
30	L32	8	31 and (438/?.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:10
31	L34	505	(438/906).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:12

	L #	Hits	Search Text	DBs	Time Stamp
32	L33	2145	(438/692).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:11
33	L35	38	34 and (scrub$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:12
34	L36	36	35 and (clean or cleaning)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 10:20

	L #	Hits	Search Text	DBs	Time Stamp
35	L37	953	(438/700).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 11:04
36	L39	550	(438/782).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 11:19
37	L40	226	(438/115).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/04/28 11:32

DOCUMENT-IDENTIFIER: US 20020142576 A1

TITLE: **Semiconductor** integrated circuit device and manufacturing method of **semiconductor** integrated circuit device

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Abstract Paragraph - ABTX (1):

After formation of Cu interconnections 46a to 46e each to be embedded in an interconnection groove 40 of a silicon oxide film 39 by CMP and then washing, the surface of each of the silicon oxide film 39 and Cu interconnections 46a to 46e is treated with a reducing **plasma** (ammonia **plasma**). Then, without vacuum break, a cap film (silicon nitride film) is formed continuously. This process makes it possible to improve the dielectric breakdown resistance (reliability) of a copper interconnection formed by the damascene method.

Title - TTL (1):

Semiconductor integrated circuit device and manufacturing method of **semiconductor** integrated circuit device

Continuity Related Application Date - RLFD (2):

20000721

Summary of Invention Paragraph - BSTX (2):

[0001] This invention relates to a **semiconductor** integrated circuit device and a manufacturing method thereof, in particular, a technique effective when adapted for the so-called damascene method wherein an interconnection having copper as a main conductive layer is formed by cutting a groove in an insulating film, forming a copper film to be embedded in the groove and polishing by CMP (Chemical Mechanical Polishing).

Summary of Invention Paragraph - BSTX (3):

[0002] Attendant on the recent tendency to miniaturizing an interconnection in a **semiconductor** integrated circuit device, a deterioration in the

of the p-channel type MISFETQP or the gate electrode 7 through the contact holes 20, 21 and 22.

Detail Description Paragraph - DETX (32):
[0166] As illustrated in FIGS. 6(a) and 6(b), a silicon oxide film 31 is deposited over the W interconnections 24 to 30 of the first layer. After through-holes 32 to 36 are formed in the silicon oxide film 31 by dry **etching** with a photoresist film as a mask, a plug 37 is formed inside of the through-holes 32 to 36.

Detail Description Paragraph - DETX (34):
[0168] As illustrated in FIGS. 7(a) and 7(b), a thin silicon nitride film 38 of about 50 nm thick is deposited over the silicon oxide film 31 by **plasma** CVD, followed by deposition of a silicon oxide film 39 of about 450 nm thick over the silicon nitride film 38 by **plasma** CVD. The silicon oxide film 39 and silicon nitride film 38 over the through-holes 32 to 36 are removed by dry **etching with a photoresist** film as a mask, whereby interconnection grooves 40 to 44 are formed.

Detail Description Paragraph - DETX (35):
[0169] The interconnection grooves 40 to 44 are formed by selectively **etching** the silicon oxide film 39 using the silicon nitride film 38 as an **etching** stopper and then **etching** the silicon nitride film 38. It is possible to control the depth of each of the interconnection grooves 40 to 44 with good precision by forming, in advance, the thin silicon nitride film 38 below the silicon oxide film 39 in which the interconnection grooves 40 to 44 are to be formed, stopping **etching** once at the surface of the silicon nitride film 38 and then **etching** the silicon nitride film 38.

Detail Description Paragraph - DETX (50):
[0184] Mechanical washing (pre-washing) of the polishing slurry is conducted, for example, as shown in FIG. 11. The both sides of the

substrate 1
turned within a horizontal plane are sandwiched by cylindrical brushes
121A,121B made of a porous synthetic resin such as PVA (polyvinyl alcohol) and
are washed simultaneously while turning the brushes 121A,121B within a plane
vertical to the surface of the substrate 1. Upon corrosion treatment after
pre-washing, the oxidizing agent in the polishing slurry adhered to the main
surface of the substrate 1 at the polishing treatment part 130 is removed
sufficiently by conducting pure water **scrub** washing, pure water ultrasonic
washing, pure water running water washing or pure water spin washing as needed
prior to or simultaneously with the corrosion treatment, whereby a hydrophobic
protecting film is formed under the conditions substantially free from the
action of the oxidizing agent.

Detail Description Paragraph - DETX (53):
[0187] The substrate 1 transferred to the post-washing treatment part 160 is
subjected to post-washing at once with the wet state of the surface being
maintained. In this part, **scrub** washing (or brush washing) of the surface of
the substrate 1 is carried out while supplying thereto a weakly alkaline
chemical liquid such as a washing liquid containing NH.sub.4OH to neutralize
the oxidizing agent and then, foreign particles formed upon **etching** are removed
by an aqueous solution of hydrofluoric acid fed onto the surface of the
substrate 1. Prior to or simultaneously with the **scrub** washing, the surface of
the substrate 1 can be subjected to pure water **scrub** washing, pure water
ultrasonic washing, running pure water washing or pure water spin washing or
the opposite surface of the substrate 1 can be subjected to pure water **scrub**
washing.

Detail Description Paragraph - DETX (58):
[0192] In the next place, the surface of each of the Cu

in the
groove, treating the surface of each of the first insulating film and interconnection with a **plasma** of reducing atmosphere, and continuously
depositing a second insulating film over the first insulating film and
interconnection while maintaining a pressure-reduced or inactive condition
without exposing the **semiconductor** substrate to the atmosphere.

Summary of Invention Paragraph - BSTX (35):
[0033] 1. A manufacturing method of a **semiconductor** integrated circuit
device, which comprises:

Summary of Invention Paragraph - BSTX (36):
[0034] (a) forming a first insulating film over a **semiconductor** substrate
and forming a groove in the first insulating film,

Summary of Invention Paragraph - BSTX (39):
[0037] (d) treating the surface of each of the first insulating film and
interconnection with a **plasma** of reducing atmosphere, and

Summary of Invention Paragraph - BSTX (40):
[0038] (e) after completion of the **plasma** treating step, depositing a second
insulating film over the first insulating film and interconnection.

Summary of Invention Paragraph - BSTX (41):
[0039] 2. A manufacturing method according to the item 1, wherein the
plasma of reducing atmosphere is an ammonia (NH.sub.3) **plasma** or hydrogen
(H.sub.2) **plasma**.

Summary of Invention Paragraph - BSTX (42):
[0040] 3. A manufacturing method according to the item 1, wherein the
plasma of reducing atmosphere is mixed gas **plasma** of ammonia (NH.sub.3) and a
diluting gas, and the diluting gas contains one or more gases selected from
hydrogen (H.sub.2), nitrogen (N.sub.2), argon (Ar) and helium (He)

Summary of Invention Paragraph - BSTX (44):
[0042] 5. A manufacturing method according to the item 1, wherein the
plasma of reducing atmosphere is a mixed gas **plasma** of hydrogen

(H.sub.2) and a
diluting gas and the diluting gas contains one or more gases selected from
ammonia (NH.sub.3), nitrogen (N.sub.2), argon (Ar) and helium (He).

Summary of Invention Paragraph - BSTX (48):
[0046] 9. A manufacturing method according to the item 8, wherein the
plasma of reduced atmosphere is an ammonia (NH.sub.3) **plasma** or a hydrogen
(H.sub.2) **plasma,** or a mixed gas **plasma** thereof with one or more gases selected
from nitrogen (N.sub.2), argon (Ar) and helium (He).

Summary of Invention Paragraph - BSTX (53):
[0051] 14. A manufacturing method according to the item 12, wherein the
plasma of reduced atmosphere is an ammonia (NH.sub.3) **plasma** or a hydrogen
(H.sub.2) **plasma,** or a mixed gas **plasma** thereof with one or more gases selected
from nitrogen (N.sub.2), argon (Ar) and helium (He).

Summary of Invention Paragraph - BSTX (58):
[0056] 19. A manufacturing method according to the item 18, wherein the
plasma of reduced atmosphere is an ammonia (NH.sub.3) **plasma** or a hydrogen
(H.sub.2) **plasma,** or a mixed gas **plasma** thereof with one or more gases selected
from nitrogen (N.sub.2), argon (Ar) and helium (He)

Summary of Invention Paragraph - BSTX (61):
[0059] 22. A manufacturing method of a **semiconductor** integrated circuit
device, which comprises:

Summary of Invention Paragraph - BSTX (62):
[0060] (a) forming a first insulating film over a **semiconductor** substrate
and forming a groove in the first insulating film,

Summary of Invention Paragraph - BSTX (65):
[0063] (d) subjecting the surface of each of the first insulating film and
interconnection to reducing treatment and nitriding treatment with a **plasma,**
and

Summary of Invention Paragraph - BSTX (67):

to occur
owing to an increase in the deposit of an organic matter by the nitrogen **plasma**
treatment as is apparent from FIG. 26 or FIG. 27.

Detail Description Paragraph - DETX (95):
[0229] Treatment is not limited to that with a single gas such as ammonia or
hydrogen but with a mixed gas **plasma** with an inactive gas such as nitrogen,
argon or helium. More specifically, a mixed gas of ammonia with hydrogen,
nitrogen, argon or helium or that of hydrogen with ammonia, nitrogen, argon or
helium can be employed. In addition, a mixed gas including three or more gases
selected from the above-described ones may be used. The amount of hydrogen,
ammonia or hydrogen+ammonia must be at least 5% of the total flow rate (mass
flow rate).

Detail Description Paragraph - DETX (101):
[0235] Downstream of the polishing treatment part 401, a post-washing part
402 is disposed for **scrub** washing of the surface of the substrate 1 which has
finished preliminary washing. The post-washing part 402 is equipped with a
loader 408, first washing part 409A, second washing part 409B, spin drier 410
and unloader 411. The post-washing part 402 is surrounded by a shading wall
430 to prevent the surface of the substrate 1 from being exposed to light
during washing and its inside is dark with an illuminance of 180 lux,
preferably 100 lux or less. This shading wall is disposed because, if the
substrate 1 having a polishing liquid attached to the surface thereof is
exposed to light under wet condition, a short-circuit current passes through
the pn junction by the photoelectromotive force of silicon, and Cu ions are
dissociated from the surface of the Cu interconnection connected to the p side
(+side) of the pn junction, which causes corrosion of the interconnection.

Detail Description Paragraph - DETX (118):

[0252] On the surface of the substrate 1 having Cu-embedded interconnections 46a to 46e formed thereon, the slurry residue containing particles such as abrasive grains or metal particles such as Cu oxide has been attached. In order to remove this slurry residue, the substrate 1 is washed with BTA-containing pure water in the clean station 404 as shown in FIG. 34. At this time, megasonic washing wherein high-frequency vibration of 800 kHz or greater is applied to the washing liquid to release the slurry residue from the surface of the substrate 1 may be used in combination. Then, the substrate 1, which is maintained under a wet condition to prevent surface drying, is transported from the polishing treatment part 401 to the post-washing part 402. In the first washing part 409A, the substrate 1 is subjected to **scrub** washing with a washing liquid containing 0.1 wt. % of NH.sub.4OH, followed by **scrub** washing with pure water in the second washing part 409B. As described above, the post-washing part 402 is covered with a shading wall 430 to prevent corrosion of the Cu interconnections 46a to 46e due to exposure of the surface of the substrate 1 to light during washing.

Detail Description Paragraph - DETX (119):
[0253] After completion of the **scrub** washing (post-washing), the substrate 1 is dried by a spin drier 410 and then transported to the subsequent step.

Detail Description Paragraph - DETX (120):
[0254] The steps after the **scrub** washing are similar to those of Embodiment 1. FIG. 43 illustrates the whole flow chart of the above-described formation process of the Cu interconnections 46a to 46e.

Detail Description Paragraph - DETX (121):
[0255] According to this embodiment, the TDDB characteristics can be improved more than that of Embodiment 1. FIG. 44 is a graph illustrating TDDB and that of this embodiment is shown by Line E. For reference, TDDB

of HF
washing. For the citric acid washing, brush **scrub** washing can be employed and
it can be conducted under the conditions of a citric acid concentration of 5%
and washing time for 45 seconds.

Detail Description Paragraph - DETX (127):
[0261] By the HF or citric acid washing, the surface layer damaged by CMP or
the like can be removed, which improves the TDDB characteristics. FIG. 46 is a
graph illustrating TDDB, wherein Line H shows the data of citric acid washing,
while Line I shows the data of HF washing, each according to this embodiment.
For reference, the data without treatment (Line Ref) and that of Embodiment 1
(Line A) are shown on the same graph. As apparent from Line J, the TDDB
characteristics show an improvement only by the HF washing without ammonia
plasma treatment, which is presumed to result from an improvement in the
properties of the interface by the removal of the damaged layer.

Detail Description Paragraph - DETX (129):
[0263] FIGS. 47 to 49 are a plan view and cross-sectional views illustrating
a manufacturing method of a **semiconductor** integrated circuit device according
to Embodiment 4 of the present invention. In FIGS. 47 to 49, only an interconnection part is shown.

Detail Description Paragraph - DETX (131):
[0265] Then, a silicon nitride film 504 and a silicon oxide film 505 of a
low dielectric constant are formed, followed by the formation of a silicon
oxide film (TEOS oxide film) 506 by the **plasma** CVD by using TEOS as a raw
material gas.

Detail Description Paragraph - DETX (132):
[0266] The silicon oxide film 505 of a **low dielectric** constant is made of a
silicon oxide insulating film having a specific dielectric constant (.di-elect
cons.) not greater than 3.0, for example, coating type insulating film such as